

Fig. 1

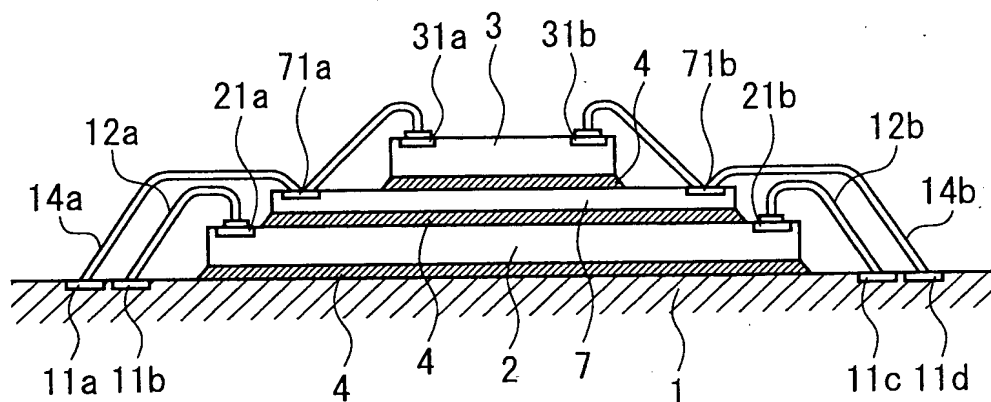


Fig. 2

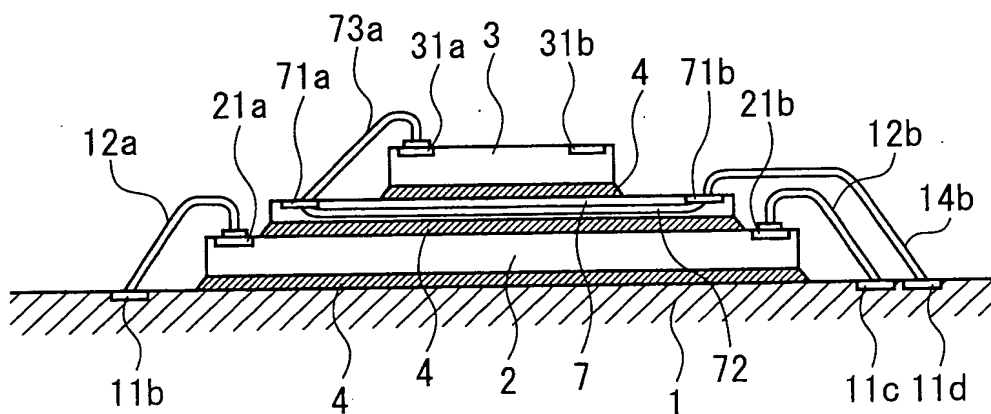


FIG. 1

Fig. 3

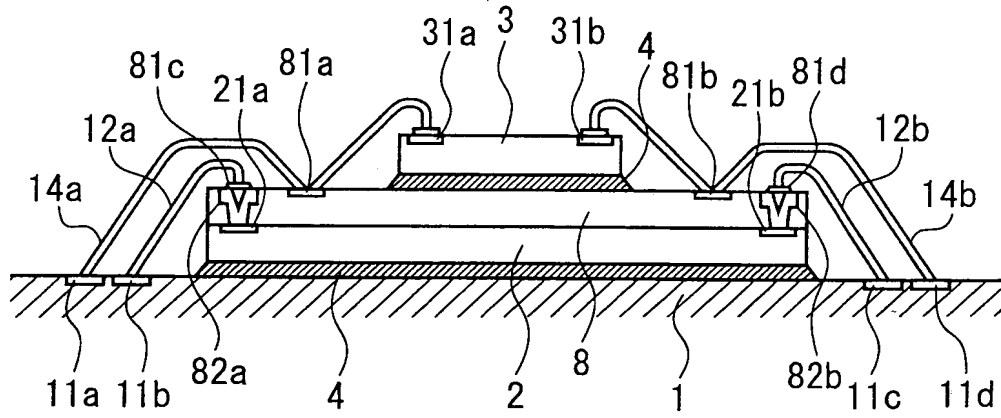
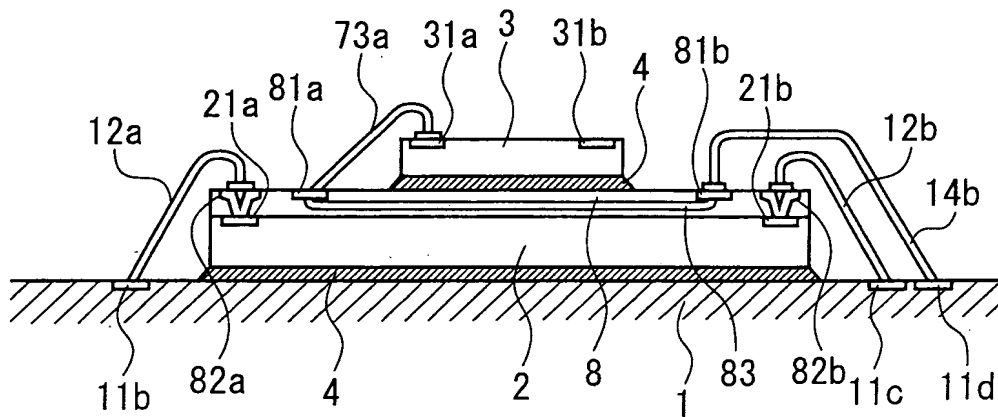


Fig. 4



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A cross-sectional view of a semiconductor device 100. The device is built on a substrate 1. A base layer 2 is formed on the substrate. A central region 3 is defined by a patterned layer 3a and 3b. A layer 4 is formed on the base layer 2. A layer 5 is formed on the central region 3. A layer 11a and 11d are formed on the substrate 1. A layer 14a and 14b are formed on the substrate 1. A layer 21a and 21b are formed on the layer 4. A layer 31a and 31b are formed on the layer 5.

A cross-sectional view of a semiconductor device 100. The device is built on a substrate 1. A base layer 2 is formed on the substrate. A gate stack 3 is formed on the base layer, with gate electrodes 31a and 31b. A channel layer 4 is formed on the base layer, with a channel region 22. A source/drain region 21a is formed on the left side, and a source/drain region 21b is formed on the right side. A contact layer 5 is formed on the source/drain regions. A wiring layer 14b is formed on the contact layer, with a contact pad 11d. A protective layer 73a is formed on the top surface of the device.

Fig. 7  
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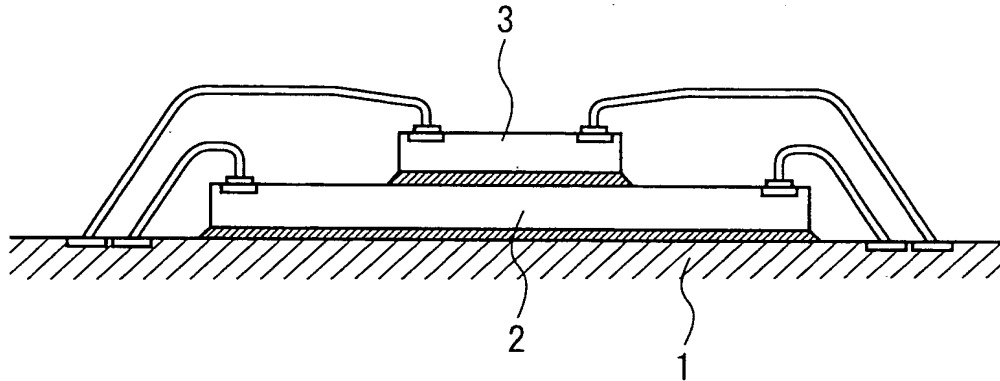
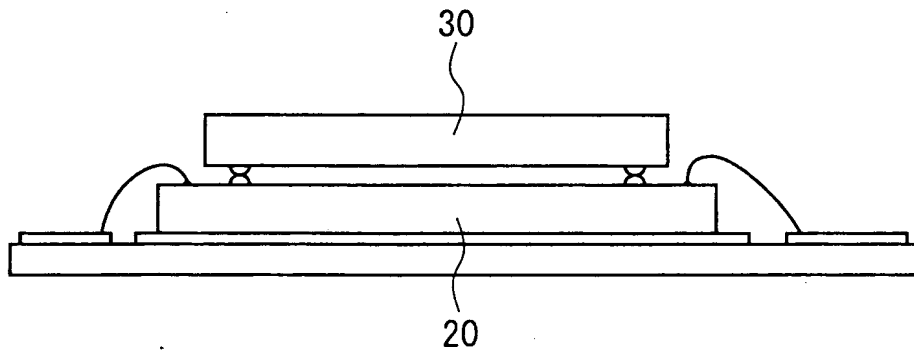


Fig. 8  
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